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09/667,528	09/22/2000	Raimund Sonning	2789-26	9877

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EXAMINER
BAYARD, EMMANUEL

ART UNIT	PAPER NUMBER
2631	5

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

20

Office Action Summary	Application No.	Applicant(s)
	09/667,528	SONNING ET AL.
	Examiner	Art Unit
	Emmanuel Bayard	2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-22* is/are rejected.

7)☒ Claim(s) *9,10,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: in line 8, replace "the" with ---a---. Appropriate correction is required.

2. Claims 9-10 are objected to because of the following informalities: in line 10, replace "the" with ---a--- , respectively . Appropriate correction is required.

3. Claim 14 is objected to because of the following informalities: in line 7, replace "the" with ---a---. Appropriate correction is required.

4. Claims 20-24 are objected to because of the following informalities: in line 26, replace "the" with ---a---, respectively. Appropriate correction is required.

5. Claims 23-24 are objected to because of the following informalities: in line 57, replace "the" with ---a---, respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 12 recites the limitation "said decoded code" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

10. Claims 1-8, 11-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Hatakeyama U.S. Patent No 6,507,629 B1.

As per claims 1, 13, Hatakeyama teaches an interleaver for interleaving input data bit sequences (BS) of M data bits comprising code symbols each consisting of a number N of data bits and control information consisting of a number L of control bits indicating specific states for

each code symbol comprising: a CRC generator for adding is similar to the claimed (combining means for combining) (see fig.4 element 20 and col.7, lines 40-67 and col.8, lines 7) the respective data bits of each code symbol with the associated L control bits into a control information/ code symbol data word of L + N bits; convolutional coder is similar to the claimed (control information/code symbol **encoding means**) (see fig.4 element 21 and col.1, lines 35-36 and col.7, line 52 and col.8, lines 16-41) for encoding said L + N bit control information/code symbol data words into data words of K bits, where K<L + N, according to a predetermined encoding scheme; an interleaving memory for storing (see fig.4 element 22 and col.8, lines 42-67 and col.9, lines 6-7, 19-20) said encoded data words at memory locations thereof.

As per claims 2, 8, 14, the interleaver of Hatakeyama does teach write/read means in row and column directions (see abstract and figs.8, 9, 14, 17 elements 51, 52, 6, 10 and col.12, lines 48-55 and col.14, lines 10, 22 and col.15, line 48 and col.17, lines 15-20 and col.21, lines 53-58 and col.22, lines 2-6, 21-25) and symbol decoding means (see fig.4 elements 13, 27 and col.9, line 41 and col.10, line 12). Note that a matrix is known in the art as function having Rows and column. Since the interleaver of Hatakemaya teaches Rows and column therefore the interleaving matrix is inherently taught by Hatakemaya.

As per claim 3, the interleaving of Hatakemaya does teach a frame start , a power bit (see col.3, lines 52-69 and col.24, lines 17-20, 50-55). Note that a frame is known in the art as plurality of time slot having a header, a maker. Since Hatakemaya teaches a frame function therefore the time slot start and the marker is inherently taught by Hatakemaya.

As per claim 4, the interleaver of Hatakemaya teaches a power bit (see col.24, lines 17-20, 50-55). Therefore a transmission power on/off is inherently includes in Hatakemaya.

As per claim 5, the interleaver of Hatakemaya does teach a selection means of write/read means (see figs. 8, 18 elements 6, 10, 151).

As per claim 6, the interleaver of Hatakemaya does teach a convolutional encoding having a coding rate (see fig.4 element 106 and col.8, lines 16-22).

As per claim 7, the interleaver of Hatakemaya does teach interleaving memory having number of rows and columns (see abstract and figs.12-16, 19-22 and col.12, lines 48-55 and col.14, lines 10, 22 and col.15, line 48 and col.17, lines 15-20 and col.21, lines 53-58 and col.22, lines 2-6, 21-25).

As per claim 11, Hatakemaya teaches a transmitter for transmitting a data bit sequence of M data bits comprising code symbols each consisting of a number N of data bits and control information consisting of a number L of control bits indicating specific states for each code symbol comprising: a CRC generator for adding is similar to the claimed (combining means for combining) (see fig.4 element 20 and col.7, lines 40-67 and col.8, lines 7) the respective data bits of each code symbol with the associated L control bits into a control information/ code symbol data word of L + N bits; convolutional coder is similar to the claimed (control information/code symbol **encoding means**) (see fig.4 element 21 and col.1, lines 35-36 and col.7, line 52 and col.8, lines 16-41) for encoding said L + N bit control information/code symbol data words into data words of K bits, where K<L + N, according to a predetermined encoding scheme; processing

means (IL, Mod) an interleaving (IL) memory for storing and modulates (see fig.4 elements 22 and 108 and col.1, lines 43-45 and col.6, lines 48-50 and col.8, lines 42-67 and col.9, lines 6-7, 19-20 and col.24, lines 42-43) said encoded data words at memory locations thereof.

As per claim 12, the transmitter of Hatakemaya does teaches a modulation means (see col.24, lines 42-43).

As per claim 15, the method of Hatakemaya does include a processing decoded code symbols (see fig.4 element 13).

As per claim 16, the interleaving of Hatakemaya does teach a frame start , a power bit (see col.3, lines 52-69 and col.24, lines 17-20, 50-55). Note that a frame is known in the art as plurality of time slot having a header, a maker. Since Hatakemaya teaches a frame function therefore the time slot start and the marker is inherently taught by Hatakemaya.

As per claim 17, the interleaver of Hatakemaya teaches a power bit (see col.24, lines 17-20, 50-55). Therefore a transmission power on/off is inherently includes in Hatakemaya.

As per claims 18, 19 Hatakemaya teaches a method for transmitting a data bit sequence of M data bits comprising code symbols each consisting of a number N of data bits and control information consisting of a number L of control bits indicating specific states for each code symbol comprising: a CRC generator for adding is similar to the claimed (combining) (see fig.4 element 20 and col.7, lines 40-67 and col.8, lines 7) the respective data bits of each code symbol with the associated L control bits into a control information/ code symbol data word of L + N bits; convolutional coder is similar to the claimed (encoding L + N control information/code

symbol) (see fig.4 element 21 and col.1, lines 35-36 and col.7, line 52 and col.8, lines 16-41) for encoding said L + N bit control information/code symbol data words into data words of K bits, where K<L + N, according to a predetermined encoding scheme; interleaving is similar to the claimed (processing) (see fig.4 element 22 and col.8, lines 42-67 and col.9, lines 6-7, 19-20) said code symbols of said encoded data words in accordance with control information; transmitting said processing code symbols (see fig.4 element 108 and col.1, lines 43-45 and col.6, lines 48-50 and col.24, lines 42-43).

As per claim 20, Hatakemaya teaches an interleaver for interleaving a data bit sequence of M data bits comprising code symbols each consisting of a number N of data bits and control information consisting of a number L of control bits indicating specific states for each code symbol comprising: a CRC generator for adding is similar to the claimed (combining means for combining) (see fig.4 element 20 and col.7, lines 40-67 and col.8, lines 7) the respective data bits of each code symbol with the associated L control bits into a control information/ code symbol data word of L + N bits; convolutional coder is similar to the claimed (control information/code symbol **encoding means**) (see fig.4 element 21 and col.1, lines 35-36 and col.7, line 52 and col.8, lines 16-41) for encoding said L + N bit control information/code symbol data words into data words of K bits, where K<L + N, according to a predetermined encoding scheme; an interleaving (IL) memory for storing(see fig.4 element 22 and col.1, lines 43-45 and col.6, lines 48-50 and col.8, lines 42-67 and col.9, lines 6-7, 19-20 and col.24, lines 42-43) said encoded data words at memory locations thereof; a write/read means in row and column directions (see abstract and

figs.8, 9, 14, 17 elements 51, 52, 6, 10 and col.12, lines 48-55 and col.14, lines 10, 22 and col.15, line 48 and col.17, lines 15-20 and col.21, lines 53-58 and col.22, lines 2-6, 21-25) for writing encoded data words. Note that a matrix is known in the art as function having Rows and column. Since the interleaver of Hatakemaya teaches Rows and column therefore the interleaving matrix is inherently taught by Hatakemaya and symbol decoding means (see fig.4 elements 13, 27 and col.9, line 41 and col.10, line 12) for decoding said K bit data words.

As per claims 21 and 22, Hatakemaya teaches an interleaver for interleaving a data bit sequence of M data bits comprising code symbols each consisting of a number N of data bits and control information consisting of a number L of control bits indicating specific states for each code symbol comprising: a CRC generator for adding is similar to the claimed (combining means for combining) (see fig.4 element 20 and col.7, lines 40-67 and col.8, lines 7) the respective data bits of each code symbol with the associated L control bits into a control information/ code symbol data word of L + N bits; convolutional coder is similar to the claimed (control information/code symbol **encoding means**) (see fig.4 element 21 and col.1, lines 35-36 and col.7, line 52 and col.8, lines 16-41) for encoding said L + N bit control information/code symbol data words into data words of K bits, where K<L + N, according to a predetermined encoding scheme; an interleaving (IL) memory for storing(see fig.4 element 22 and col.1, lines 43-45 and col.6, lines 48-50 and col.8, lines 42-67 and col.9, lines 6-7, 19-20 and col.24, lines 42-43) said encoded data words at memory locations thereof; a write/read means in row and column directions (see abstract and figs.8, 9, 14, 17 elements 51, 52, 6, 10 and col.12, lines 48-55 and col.14, lines 10, 22 and

col.15, line 48 and col.17, lines 15-20 and col.21, lines 53-58 and col.22, lines 2-6, 21-25) for writing encoded data words. Note that a matrix is known in the art as function having Rows and column. Since the interleaver of Hatakemaya teaches Rows and column therefore the interleaving matrix is inherently taught by Hatakemaya and symbol decoding means (see fig.4 elements 13, 27 and col.9, line 41 and col.10, line 12) for decoding said K bit data words according to an inverse predetermined coding scheme and wherein each memory location (see figs.8, 17 elements 2, 3 and col.11, lines 15-67) stores one data word respectively consisting of said encoded combination of a predetermined number n of data selected from an input data bit sequence by a selection means of said write/read means (see figs. 8, 17 elements 6, 10 and col.11, lines 15-67 and col.12, lines 3-67) and said control bits (see figs.8, 17 element 4 and col.11, lines 19-20, 28-30, 36-37).

Allowable Subject Matter

11. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 23-24 are objected, but would be allowable if rewritten to overcome the above objection.

13. The following is a statement of reasons for the indication of allowable subject matter: a shift means for shifting the register (ro, r1) which was read at the last write cycle and the second registers of the register banks (b0, b1) while reading in the next odd and even bits of a next input data bit sequence to the respective second register (r1) of each register bank as recited in claims 8-10 and 23-24.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gray U.S. Patent No 6,597,526 B1 teaches a magnetic tape drive apparatus.

Lim et al U.S. Patent No 6,182,265 B1 teaches a method for encoding a channel using parallel convolutional encoder.

Benson et al U.S. Patent No 5,907,566 teaches a continuous byte-stream encoder/decoder.

Gray U.S. Patent No 5,815,514 teaches a variable rate bit inserter.

Zehavi U.S. Patent No 6,553,538 B2 teaches a method and apparatus for providing error protection.

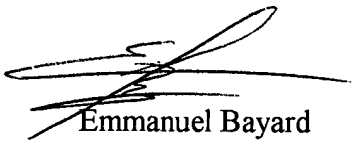
St. John et al U.S. Patent No 5,892,464 teaches a message encoding technique.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is (703) 308-9573. The examiner can

normally be reached on Monday-Thursday from 8:00 AM - 5:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour , can be reached on (703) 306-3034. The fax phone number for this Group is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3800.



Emmanuel Bayard

Primary Examiner

August 13, 2003